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Characteristics of solid-phase diffused ultra-shallow junction using phosphorus doped silicon oxide films for fabrication of sub-100 nm SOI MOSFET

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Strenuous efforts are being focused on further scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) into the sub-100 nm regime. Complementary MOS devices (CMOS) fabricated on silicon-on-insulator (SOI) wafers have attracted a lot of attention because of the advantages of full dielectric isolation and reduced junction capacitance over those on bulk silicon wafers in regard to integrated circuit (IC) applications for low stand-by power and high performance. Moreover, the fabrication technique involved in SOI MOSFET can remove or relax some of the process and material constraints on the MOSFET scaling, because it provides a low leakage current, latch-up elimination, high soft error immunity, smaller subthreshold swing, and a simple device structure and process. However, one of the major challenges to overcome is the ultra-shallow junction formation method, which prevents short channel effects for deep sub-100 nm devices [1, 2]. The conventional approach for junction formation is ion implantation with low-energy ion beams. The crystal defects associated with the energetic ion beam bombardment are unavoidable and act as the primary source of junction leakage currents. The junction leakage degrades the device performance and leads to an increase in power consumption. Therefore, an alternative method is required to make use of the advantages of the SOI devices. Doping using solid-phase diffusion (SPD) is an effective method to form damage-free ultra-shallow junctions.

In this paper, we report the doping properties of the SPD method and the electrical characteristics of sub-100 nm SOI MOSFETs fabricated using the SPD technique for ultra-shallow source and drain junction formation. The phosphorus doped oxide films used as the SPD source are usually prepared by chemical vapor deposition (CVD), but we used a liquid-state dopant source containing silicon, oxygen and phosphorus. A wafer was coated with the dopant source using a spin coating technique. After baking at 250 °C for 20 min, the liquid source was converted to a solid phosphorus doped silicon oxide layer on the top of the wafer. The refractive index and density of this oxide layer were 1.42 and 2.05 g/cm^3, respectively. Then the coated wafer was placed in a rapid thermal annealing (RTA) system and a PN junction was created after the phosphorus had diffused into the silicon. In this way, N^+P junction diodes and SOI MOSFETs were fabricated.

Fig. 1 shows the secondary ion mass spectrometry (SIMS) depth profile of phosphorus for various RTA process temperatures. The RTA process was performed for 30 s in N_2 ambient. The diffusion depth of the phosphorus increases with RTA temperature. The surface concentration of phosphorus also increased with the RTA temperature due to the enhanced solid solubility of phosphorus atoms. In nano-scale MOSFET devices, a channel impurity concentration of 10^{18} cm^{-3} is required to suppress the short channel effect. It is clear that a shallow junction, less than the 50 nm deep, defined at 1×10^{18} cm^{-3} can be obtained when the RTA temperature is below 925 °C.

Fig. 2 shows the relationship between the sheet resistance (Rs) measured using the four-point probe and RTA temperature. The Rs monotonically decreases as the RTA temperature and junction depth increase. The Rs is lower than 1 k Ohm/cm^2 at 925 °C, which is the maximum drain extension sheet resistance required for 32 nm-technology [3]. Since the surface dopant concentration increased as the RTA temperature increased, more improvements can be expected with control of RTA duration time.

Fig. 3 shows the current-voltage (I-V) characteristics of N^+P diodes fabricated on SOI substrates by SPD methods. In order to verify the effectiveness of the SPD process, the I-V characteristics of N^+P diodes fabricated by the plasma doping method, which is often used in ultra-shallow junction formation, are also shown in Fig. 3 for comparison. It is observed that the forward bias current depends on the RTA temperature. As the RTA temperature increased, the forward bias current increased, while the reverse bias current remained almost constant. The increase in forward bias current could be attributed to the reduction of sheet resistance resulting from high temperature RTA. In the case of the plasma doping sample, the forward bias cur-

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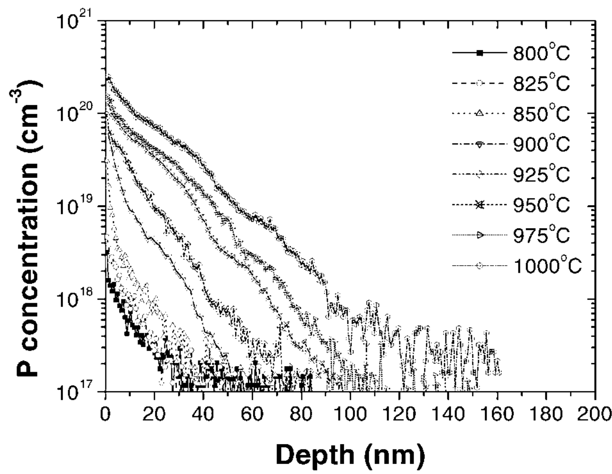


Figure 1 Depth profiles of *P* analyzed by SIMS for various RTA temperatures.

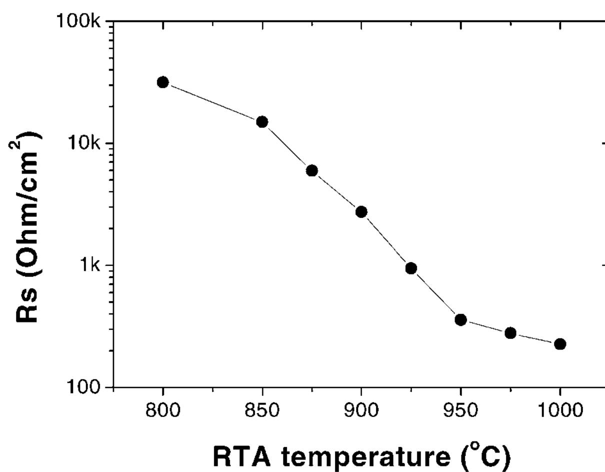


Figure 2 Dependence of sheet resistance (Rs) on RTA temperature.

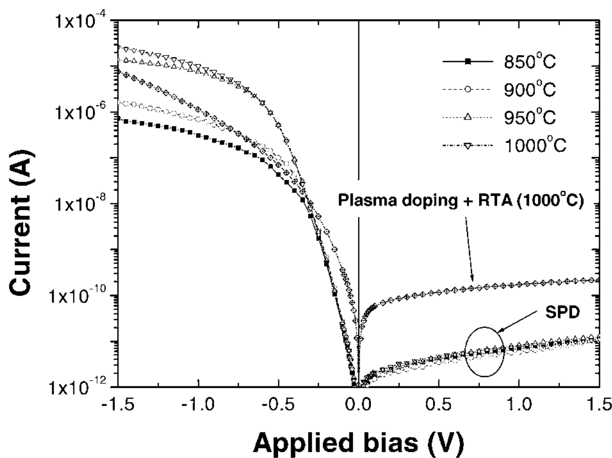
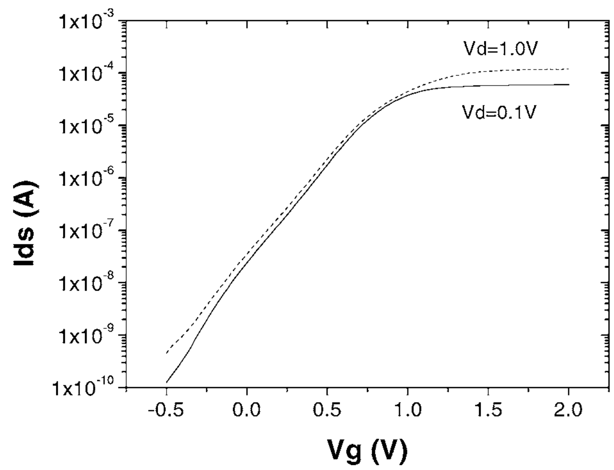


Figure 3 Current-voltage characteristics of N^+P diode using SPD method and plasma doping method.

rent is lower and the reverse bias is higher than those of the SPD samples even after annealing at 1000 °C. It is well known that defects generated by ion implantation or plasma doping cannot be completely annealed out [4]. The SPD method does not create the defects during the junction formation. Consequently, these results clearly show that the SPD process is superior to the plasma doping process for diode formation.



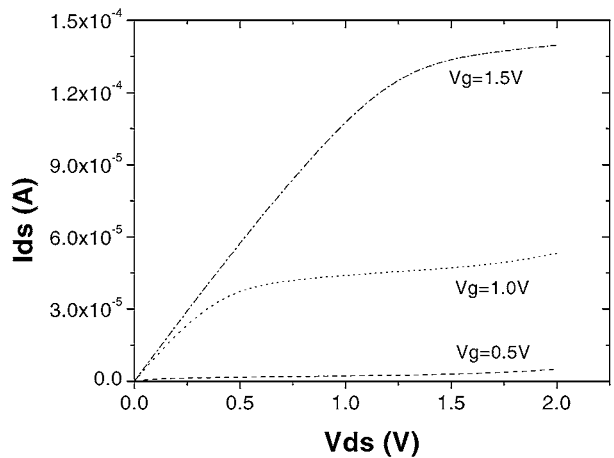


Figure 4 I_D-V_G, I_D-V_D characteristics of SOI MOSFET fabricated by SPD method ($L_g = 0.1\ \mu$m/$W_{ch} = 2\ \mu$m).

Fig. 4 shows the subthreshold characteristics (I_d-V_g) and the measured drain current (I_d-V_d) for the SOI N-MOSFET of 0.1 um gate length and 2 um channel width without gate spacer and LDD (lightly doped drain) structure, which was fabricated by the SPD method with 950 °C RTA. It has an excellent subthreshold behavior on/off current ratio. These results confirm that the SOI N-MOSFET fabricated by SPD method with spin coated oxide glass operated successfully, providing a promising doping method to make sub-100 nm MOSFETs.

In summary, the solid-phase diffusion (SPD) method for an ultra-shallow junction formation has been investigated. Sheet resistances of the phosphorus diffused area were below 1 k Ohm/cm^2 when the RTA temperature was higher than 925 °C. The diffusion depth of the phosphorus could be controlled to be below 40 nm with temperatures lower than 925 °C. The diode characteristics of N^+P junction were improved as the RTA temperature was increased and a comparison study shows that the SPD method is superior to the plasma doping method. SOI N-MOSFETs fabricated by this SPD method operated successfully, demonstrating SPD to be a promising doping technique.

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